The Reliability Analysis and Structure Design for the Fine Pitch Flip Chip BGA Packaging

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Abstract
The flip chip packaging structure design and the fabrication process parameters will influence the packaging reliability and the performance of chip heat dissipation. The reliability of a flip chip package depends on the packaging structure design parameters, which include solder bump geometry, die side pad and substrate side pad dimensions, etc. In order to study the effects of bonding pad size and solder bump geometry for the flip chip packaging reliability, three different structures of the fine pitch flip chip BGA packages including daisy chain circuit are designed, fabricated and tested in this investigation for the parametric analysis. Subsequently, the analytical solution analyzing technique for solder joint shape prediction is employed in this study for the preliminary prediction of package reliability. Furthermore, a finite element method (FEM) is also applied for the packaging reliability analysis. The findings depict that the packaging structure with better solder bump shape shows better reliability, and the trends of reliability testing and FEM results coincide with the analytical solution of the solder shape prediction.

Keywords: Parametric analysis, Flip chip BGA, Reliability, Daisy chain, and Finite element method.

Ⅰ. Introduction

The flip chip packaging technology has widely been used in modern electronics packaging industry due to its good thermal performance, smaller size, lower profile, lighter weight, and higher I/O density. Normally, the key factors, which influence a package's reliability are the geometry of the solder joint, underfill material, solder material, as well as its geometrical and structural configuration. These reliability analyses of flip chip packaging have been subjected to substantial research for the past years.

The solder joint reliability has been found [1, 2] to be highly dependent on solder joint geometry such as standoff height, lower/upper contact angles of solder joint, solder pad diameter and solder shape, etc. Among the solder shape prediction algorithms, Chiang (1998) [3] as well as Heinrich et al. (1996) [4] have developed prediction models for the area array type solder joints on the basis of force-balanced analytical algorithms and Pfeifer [5] produced a geometrical based algorithm-truncated sphere method, which does not take any force or energy factors into consideration.

Popelar [6] studied the reliability of flip chip package based on the finite element method (FEM) parametric analysis. The results could be divided into two parts: one indicates that the flip chip packages without underfill show worse reliability, and the design parameters such as die size, solder bump height and pad diameter obviously influence the reliability of flip chip package without underfill. The other result indicates that the flip chip packages with underfill show better reliability, but die size, solder bump height and pad diameter show smaller influence to the reliability. Mercado [7, 8] applied FEM parametric analysis to study the reliability of flip chip PBGA, and the design parameters including solder bump layout, solder bump center to die edge, solder material/geometry, die size as well as substrate size/material.

About the flip chip package fabrication and reliability testing, Chen [9] investigated the test methodology for assessing reliability performance of both single chip and multiple chips flip chip on board (FCOB) assemblies. Rosner et al. [10] developed a thermal cycle testing experiment for the flip chip packaging using isotropically conductive adhesives. In his research, a special daisy chained test IC is designed for the packaging reliability testing. The daisy chain electrical resistance variation is measured at different time instances of the thermal cycling, and the results indicate that the package structure failure in the thermal cycle testing may occur at both low and high temperatures.

In this study, three different structures of the fine pitch flip chip BGA packages are designed, fabricated and tested for the reliability design. The flip chip package is mounted on a 1+2+1 built-up organic substrate with 2,499 solder bumps. On the BGA side, it is mounted on the testing printed wiring board (PWB) with 664 solder balls. In order to reduce the testing time, this research applies flip chip package without underfill structure in the thermal cycle testing. Center cross-section of the flip chip BGA package without underfill is illustrated in Figure 1.

Ⅱ. Solder bump shape prediction

The truncated sphere theory and the force-balanced method are employed in this study to predict the solder bump shape for the preliminary prediction of packaging reliability. These two algorithms that show good abilities in solder joint shape prediction [11] are briefly described as follows:

A. Truncated sphere theory

In an area array package mounted on a PWB case, the

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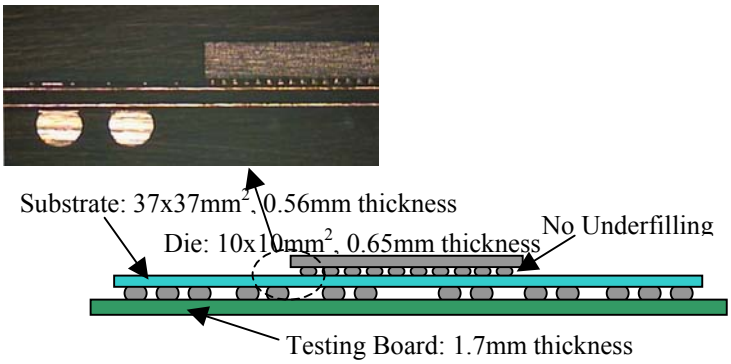


Fig. 1: Cross section view of flip chip BGA package without underfill

solder joint between the die side and substrate side assumes the of a "double truncated sphere" (Fig. 2) and the bump height h and solder diameter D can be determined by changing the solder volume V. Once the solder volume is obtained, the standoff height and the diameter of the solder bump can be predicted by (1)-(3).

$$h = \sqrt{R^2 - a^2} + \sqrt{R^2 - b^2} \tag{1}$$

$$D = \frac{\sqrt{h^4 + 2h^2(a^2 + b^2) + (a+b)^2(a-b)^2}}{h} \tag{2}$$

$$V = \frac{\pi}{12h^3}\left[C_1\left(C_1^2 + 6a^2h^2\right) + C_2\left(C_2^2 + 6b^2h^2\right)\right] \tag{3}$$
$$C_1 = \sqrt{h^4 + \left(a^2 - b^2\right)^2 - 2\left(a^2 - b^2\right)h^2}$$
$$C_2 = \sqrt{h^4 + \left(a^2 - b^2\right)^2 + 2\left(a^2 - b^2\right)h^2}$$

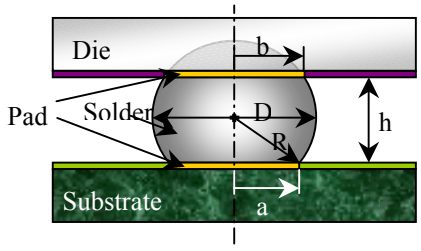


Fig. 2: Solder joint on substrate

B. Forced-balanced analytical method

Chiang (1998) [3] and Heinrich et al. (1996) [4] have addressed the close form solution of the force-balanced algorithm for solder formation. Figure 3 indicates that the package weights at the upper pad F_h should be balanced by the solder joint internal pressure and the surface tension if the solder is in the minimum energy state. A Laplace equation is applied to calculate the profiles of the solder surface, the governing equation of molten solder joint under static equilibrium can be expressed as:

$$P_0 = P_a + \gamma\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \rho g(h - z) \tag{4}$$

Where R_1 and R_2 are the principal radii of curvatures of the solder surface at height h; P_a, P_0, γ are ambient pressure, internal pressure and surface tension, respectively; the variables P, R, R_1 and R_2 are the functions of z.

For molten solder joint, the gravitational force is much smaller than surface tension. Therefore, the third term in equation (4) can be neglected and the governing equation can be simplified as:

$$P = P_0 - P_a = \gamma\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{5}$$

For axisymmetric cases, the governing equation becomes:

$$\gamma R R'' - \gamma (R')^2 + PR[1 + (R')^2]^{3/2} - \gamma = 0 \tag{6}$$

The solder volume that is a function of R(z) could be written as:

$$V = \pi \int_0^h (R)^2 dz \tag{7}$$

The unbalanced force for a molten solder joint can be expressed as:

$$\delta F = F_h - \frac{\pi R_h}{2hR} \left[\mp (R_0 + R_h) - \sqrt{\frac{4R^2h^2}{(R_0 + R_h)^2 + h^2} - h^2}\right] \tag{8}$$

An initial value of standoff height h should be assigned to iterate the unbalanced force. The standoff height h must be adjusted for further iteration if $|\delta F|$ exceeds the converging tolerance. Once the force is balanced, the approximate shape and height of the solder joint could be determined.

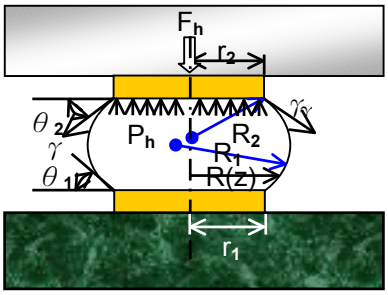


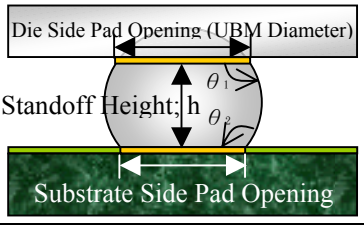
Fig. 3: Solder joint force balanced free body diagram

C. Flip chip packaging solder bump shape prediction

Based on the above solder joint shape forming theories, the flip chip solder bump shape can be calculated for the preliminary prediction of package reliability. In this investigation, there are three different package structures: MPE002, MPE003 and MPE004 as shown in Table 1.

Table1: The design parameters of three flip chip packaging structure

	MPE002	*MPE003*	*MPE004*
UBM Diameter	**80 μm**	**90 μm**	**100 μm**
Bump Height	**80 μm**	**80 μm**	**80 μm**
Substrate Side Pad Opening	**120 μm**	**120 μm**	**120 μm**



In this analysis, the die size is 10 x 10 x 0.65 mm^3, the density of silicon is 2330e-6 (g/mm^3), and solder bump counts is 2,499. Therefore, the die weight is 148.42 (dyne), and the force on each bump is 0.059 (dyne/bump). Table 2 depicts the predicted results of solder bump shapes. It can be seen in Table 2 that MPE004 shows the highest standoff height, the largest solder volume and the smallest upper contact angle.

Table 2: The prediction values of solder bump shape

MPE002	Volume (mm^3)	**0.0004691**
	Standoff Height; h (μm)	**49.4**
	Upper Contact Angle; θ_1	**139.1^0**
	Lower Contact Angle; θ_2	**95.0^0**
MPE003	Volume (mm^3)	**0.0005226**
	Standoff Height; h (μm)	**51.0**
	Upper Contact Angle; θ_1	**133.1^0**
	Lower Contact Angle; θ_2	**100.3^0**
MPE004	Volume (mm^3)	**0.0005822**
	Standoff Height; h (μm)	**52.6**
	Upper Contact Angle; θ_1	**127.0^0**
	Lower Contact Angle; θ_2	**105.5^0**

Ⅲ. Test vehicles development

A. Test vehicles

These fine pitch flip chip BGA test vehicles employed in this study use three different daisy-chained test dies (shows in Table 1). The test die size is 10 x 10 x 0.65 mm^3, 200 μm bump pitch and 2,499 I/O, and the die edge to outmost solder bump center is 120 μm. A special daisy chain circuit has been designed to investigate the reliability of flip chip BGA package. The daisy chain circuit is designed for two functions: substrate level testing and board level testing. One circuit connects all of the flip chip solder bumps to form a daisy-chained circuit for substrate level testing. Another daisy chain connects all of the BGA solder balls and interconnects with flip chip solder bumps through the substrate via to form a board level testing circuit. Figures 4 and 5 illustrate the substrate level testing and board level testing daisy chain circuit layout.

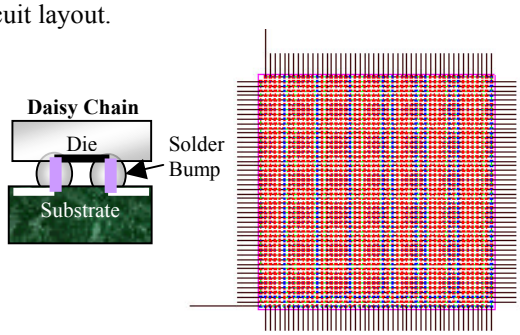


Fig. 4: Daisy chain circuit on flip chip solder bumps (Substrate level)

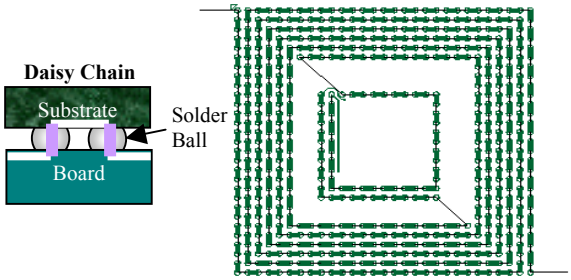


Fig. 5: Daisy chain circuit on BGA solder balls (Board level)

These packages apply a 1+2+1 built-up organic substrate. The substrate size is 37.5 x 37.5 x 0.56 mm^3, 664 ball counts, pad opening on flip chip side is 120 μm, and pad opening on BGA side is 600 μm. Figure 6 shows the substrate layout. On the four sides of the substrate are probing pads (500 x 500 μm^2) connected with the outmost solder bump, these probing pads can be applied to measure the signals of outmost solder bumps during the thermal cycle testing for flip chip solder bump array failure location judgment. The BGA side of substrate is connected to a testing board that is measured 21 cm x 12 cm x 0.17 cm^3. The testing board made by organic material has six BGA substrate attaching sites. The daisy

chain net is formed after the die, substrate, and testing board assembly.

The aluminum metal pad, daisy chain circuit on die side and circular passivation opening layer are patterned on the wafer (figure 7). The UBM layer is composed of titanium (sputtered), copper (sputtered) and nickel (electroplating). The bump material is 63Sn/37Pb eutectic solder. Figure 8 illustrates the solder bump on daisy chain wafer.

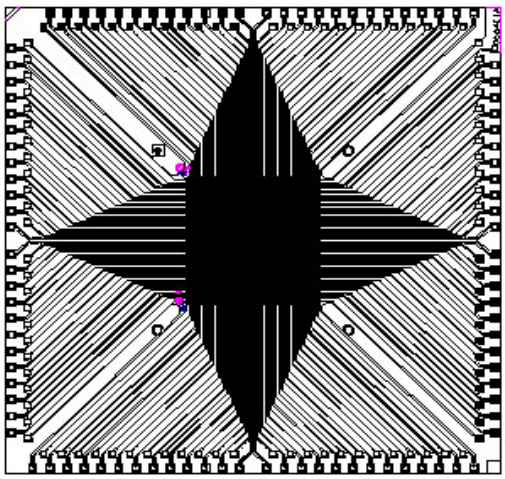


Fig. 6: Substrate layout

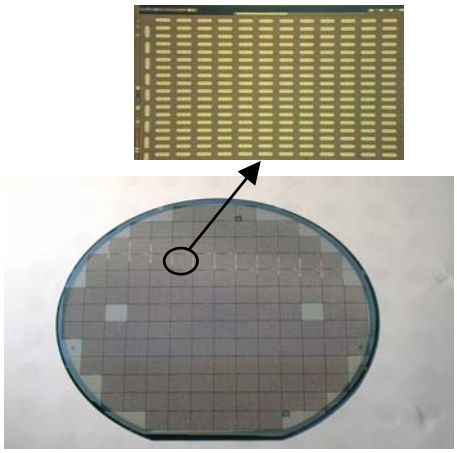


Fig. 7: Daisy chain

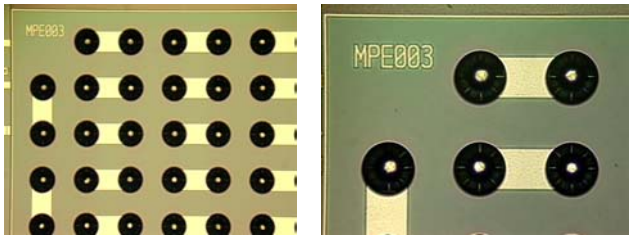


Fig. 8: Solder bump on daisy chain wafer

B. Assembly

The laminated substrates are fluxed and die are placed and aligned on the substrate by commercially available equipment. The assembled parts are reflowed through a reflow oven. To reduce the thermal cycle testing time, the underfill material does not use in the flip chip package. Figure 9 depicts the fabricated flip chip BGA package. Subsequently, the flip chip BGA package is mounted on the testing board (Fig.10). Figures 11 and 12 illustrate the BGA solder ball and flip chip solder bump, respectively. After assembly, the test vehicles are finished and the daisy chain net is formed, hence the measurements of daisy chain electrical resistance could be accomplished during thermal cycle testing.

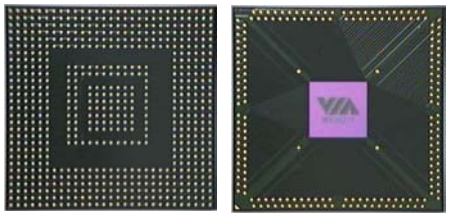


Fig. 9: The flip chip BGA package

Fig. 10: Flip chip BGA on Board

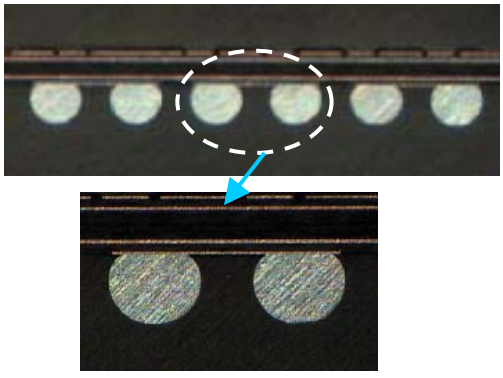


Fig. 11: BGA solder ball

Fig. 12: FC Solder bump after assembly

Ⅳ. Testing

In order to distinguish the reliability of three different flip chip packaging structures, a thermal cycle testing is employed in this investigation. Each type of testing flip chip BGA package has 24 samples on four testing boards. Due to no underfilling of the flip chip package causes the structure weakness, these samples were exposed to thermal cycling between a less harsher environment: 0^0C to 100^0C (Condition J, JEDEC). The time duration of one period is 60 minutes. The initial daisy chain resistance of the three packages is different owing to the variant structure. The initial resistance of MPE002 at room temperature is about 70 to 73 ohm, MPE003 is 74 to 78 ohm and MPE004 is 84 to 88 ohm.

The daisy chain electrical resistance variation is measured at 0^0C and 100^0C by real time monitoring test oven during the thermal cycling. The thermal mismatch between die and substrate can cause the deterioration of the solder bump interconnections. Table 3 lists the thermal cycle testing results. Figures 13 to 15 show the daisy chain resistance value variation with thermal cycle numbers of MPE002, MPE003 and MPE004 during thermal cycling.

Table 3: Thermal cycle testing results of MPE002, MPE003 and MPE004

Samples	*MPE002 (Fatigue Cycle Number)*	*MPE003 (Fatigue Cycle Number)*	*MPE004 (Fatigue Cycle Number)*
1	15	41	64
2	12	43	61
3	11	41	64
4	14	39	90
5	13	34	62
6	15	34	71
7	12	40	71
8	12	36	69
9	14	34	68
10	11	34	79
11	12	42	66
12	11	34	67
13	12	33	62
14	14	41	67
15	13	32	68
16	14	41	69
17	14	37	84
18	13	37	62
19	13	34	63
20	15	40	68
21	14	47	61
22	12	43	64
23	14	44	64
24	14	47	64
Average	**13**	**39**	**68**

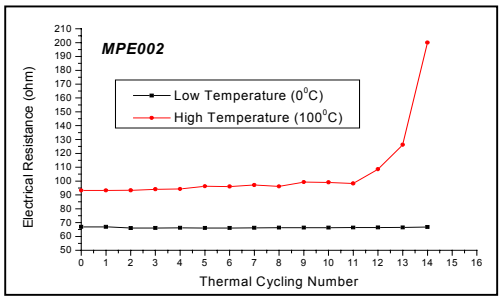


Fig. 13: Thermal cycling profile of MPE002

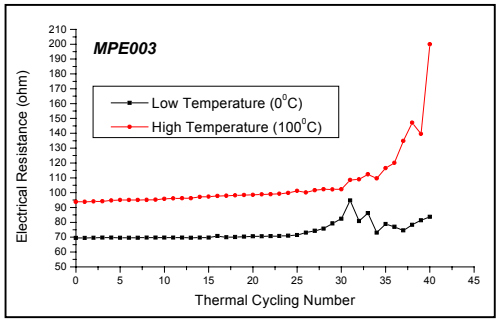


Fig. 14: Thermal cycling profile of MPE003

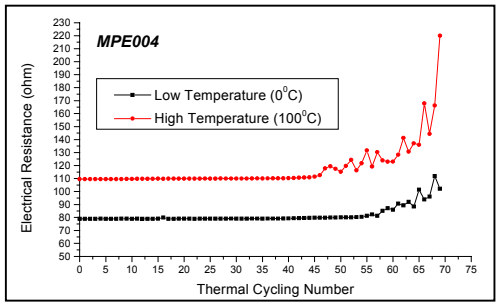


Fig. 15: Thermal cycling profile of MPE004

Ⅴ. FEM Validation

To validate the analytical solution results, the finite element method (FEM) is also applied in this study for the packaging reliability analysis. Three FEM models are employed herein to simulate the accelerated thermal cycling (ATC), as well as temperature rising and dwelling between 0^oC and $100\,^o$C.

A. Thermal fatigue life prediction

As an electronic packaging is subjected to temperature loading, the large stress/strain of a solder bump will cause the failure to the packaging structure. To predict the thermal fatigue life of the solder bump, the Coffin-Manson relationship is employed:

$$N_f = \theta\left(\Delta\gamma_p\right)^{\eta} \tag{9}$$

Where N_f is the mean cycle to failure, $\Delta\gamma_p$ is the shear strain range in one cycle of thermal loading. For eutectic solder, the average values of the constants θ and η determined by Solomon [12], θ is the coefficient of

fatigue ductility with a value of 1.2928 and η is the fatigue ductility exponent, which is -1.96. Due to the fact that the stress acting on the solder bump of the flip chip packaging is not only dominant by the shear direction, the equivalent plastic strain is applied in this study. The incremental equivalent plastic strain can be expressed as:

$$\Delta\varepsilon_{eq}^{pl} = \frac{\sqrt{2}}{3}\sqrt{\begin{aligned}&(\Delta\varepsilon_x^{pl} - \Delta\varepsilon_y^{pl})^2 + (\Delta\varepsilon_y^{pl} - \Delta\varepsilon_z^{pl})^2 \\ &+(\Delta\varepsilon_z^{pl} - \Delta\varepsilon_x^{pl})^2 + \frac{3}{2}\Delta\gamma^{pl}\end{aligned}} \quad (10)$$

Where $\Delta\gamma^{pl} = \Delta\gamma_{xy}^{pl\,2} + \Delta\gamma_{yz}^{pl\,2} + \Delta\gamma_{zx}^{pl\,2}$ and $\Delta\varepsilon_x^{pl}$ 、 $\Delta\varepsilon_y^{pl}$ 、 $\Delta\varepsilon_z^{pl}$ 、 $\Delta\gamma_{xy}^{pl}$ 、 $\Delta\gamma_{yz}^{pl}$ and $\Delta\gamma_{xz}^{pl}$ are incremental plastic strain components acting on the solder bump.

Subsequently, the fatigue life of a eutectic solder can be predicted by using a modified Coffin-Manson relationship:

$$N_f = \theta\left(\Delta\varepsilon_{eq}\right)^{\eta} \quad (11)$$

Where the constants θ and η are modified to 0.4405 and –1.96, respectively.

B. Finite element model

In this study, two-dimensional nonlinear finite element models established by the commercial software ANSYS are applied to simulate the stress/strain behavior under thermal cycle testing. A two-dimensional four-nodes element and a plane strain assumption are adopted in the analysis. Figure (16) and (17) illustrate the FEM models of MPE002, MPE003 and MPE004. It could be observed in figure 16 that an AA' cross-section is employed and a one-half model of the FCBGA is considered due to the symmetric geometry in the FEM analysis. This finite element model contains 33,400 elements and 66,800 D.O.F. The boundary condition is with one node fixed in y direction on the center of bottom side of the testing board and a symmetry condition is conducted on the X=0 line. The temperature range varies from 0^0C to 100^0C with one hour per cycle in the simulation analysis and the stress free temperature is 25^0C.

Table 4 indicates the material properties of silicon chip, copper pad, Fr-4 testing board, BT substrate and solder mask. Figure 18 depicts the temperature dependent nonlinear material properties of eutectic solder. To ensure nonlinear convergence, the full Newton-Raphson method is applied in the analysis.

Table 4: Linear material properties of the FCBGA

Material	Young's Modulus (Gpa)	Poisson's Ratio	CTE (1/℃)
Silicon	112.4	0.28	2.62ppm
Copper pad	68.9	0.34	16.7ppm
Fr-4 testing board	18	0.19	16ppm
BT substrate	9.92	0.2	15ppm
Solder mask	3.448	0.35	30ppm

C. Result

Figure 19 shows the incremental equivalent plastic strain after five thermal cycles of package MPE002, MPE003 and MPE004. It is found in figure 19 that the maximum equivalent plastic strain occurs at the outmost solder bump in three packages.

Simulation results of the FEM analysis of the packages MPE002, MPE003 and MPE004 are described below: The package MPE002 has the maximum one cycle accumulated equivalent plastic strain of 12.17% in the outermost solder bump. This strain is substituted into Coffin-Manson equation (equation 11) to obtain the mean cycle to a failure of 27 cycles. The package MPE003 has the maximum one cycle accumulated equivalent plastic strain of 8.87%. This strain is substituted into Coffin-Manson equation to obtain the mean cycle to a failure of 51 cycles. The maximum one cycle accumulated equivalent plastic strain of package MPE004 is 7.05%. Its mean cycle to a failure is 80 cycles. Figure 20 illustrates the comparison result between thermal cycling experiment and FEM simulation.

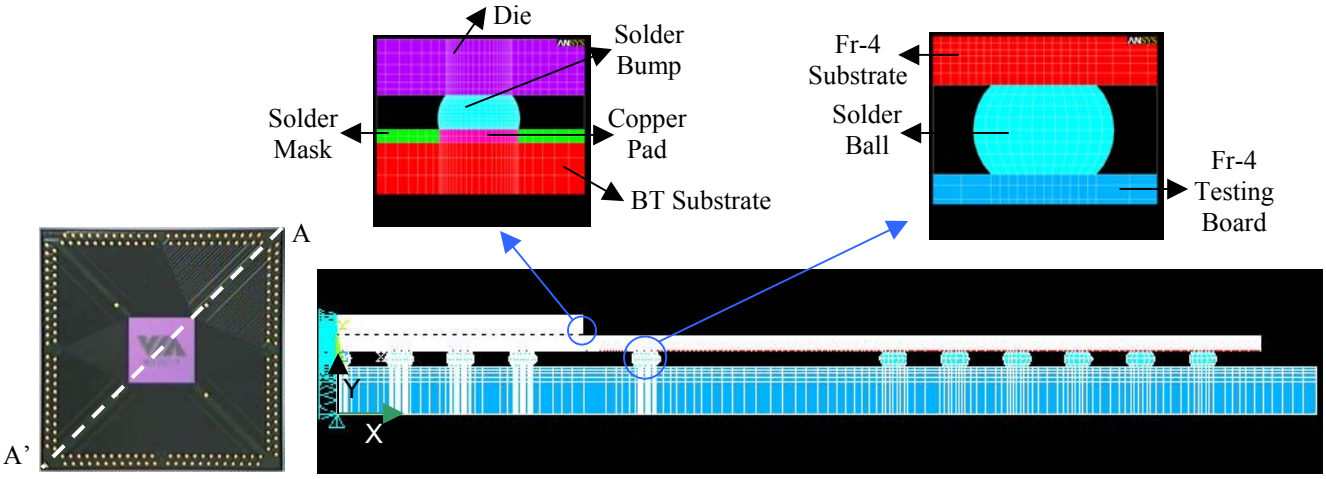
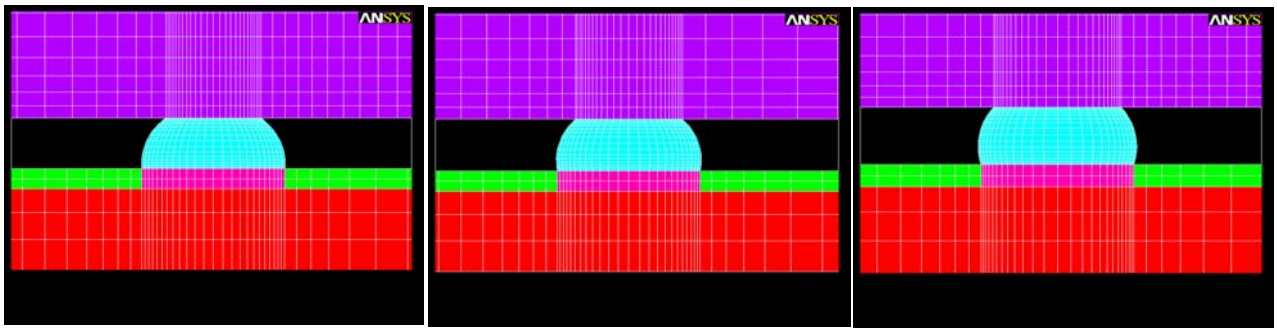


Fig. 16: Two-dimensional nonlinear finite element model



(a) (b) (c)

Fig. 17: The solder bump view of FEM model of (a) MPE002, (b) MPE003 and (c) MPE004

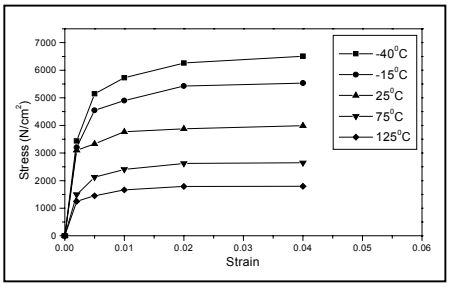


Fig. 18: The temperature dependent nonlinear material properties of eutectic solder

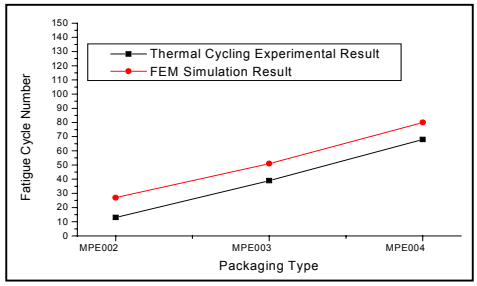


Fig. 20: The comparison result between thermal cycling experiment and FEM simulation

Although there are a few errors between FEM and thermal testing findings due to FEM model simplify (such as 2D plane strain assumption and testing vehicle simplification), it is observed that the trends of FEM results well coincide with it of experimental data.

VI. Discussion

Due to no underfilling cause the weakness of the packaging structure, these three chips show lower reliabilities than the flip chip packages with underfill. However, the reliability of MPE002, MPE003 and MPE004 still can be estimated for comparison. It could be found from table 3 as well as from figures 20 that chip MPE004 shows the best reliability in both thermal cycle testing and FEM simulation, followed by chip MPE003, and the chip MPE002 shows the worst reliability. Moreover, all these packages fail at high temperature: 100^0C. Since there is no underfilling in the packaging structure, the stress at the solder joint from CTE mismatch can not be reduced and absorbed by the underfill during thermal cycle testing, therefore the thermal cycling profiles display that the solder joint fails as the daisy chain resistance starts rising in a few cycles.

Compared to the thermal cycle testing and the FEM results with the analytical solution data illustrated in table 2, among chip MPE002, MPE003 and MPE004, the standoff height follows the relation: MPE004 > MPE003 > MPE002; the solder volume is related by: MPE004 > MPE003 > MPE002; whereas the upper contact angle shows that: MPE004 < MPE003 < MPE002. On the physical viewpoints, a solder joint with a larger solder volume, and higher standoff height can reduce the stress and strain causing from CTE mismatch between different materials; a smaller contact angle of the solder joint can avoid the stress concentration effect. According to the above physical phenomena, Chip MPE004 has a larger solder volume, a higher standoff height and a smaller contact angle; thereby it shows a better reliability. Chip MPE002 has a smaller solder volume, a lower standoff height and a larger contact angle among these three

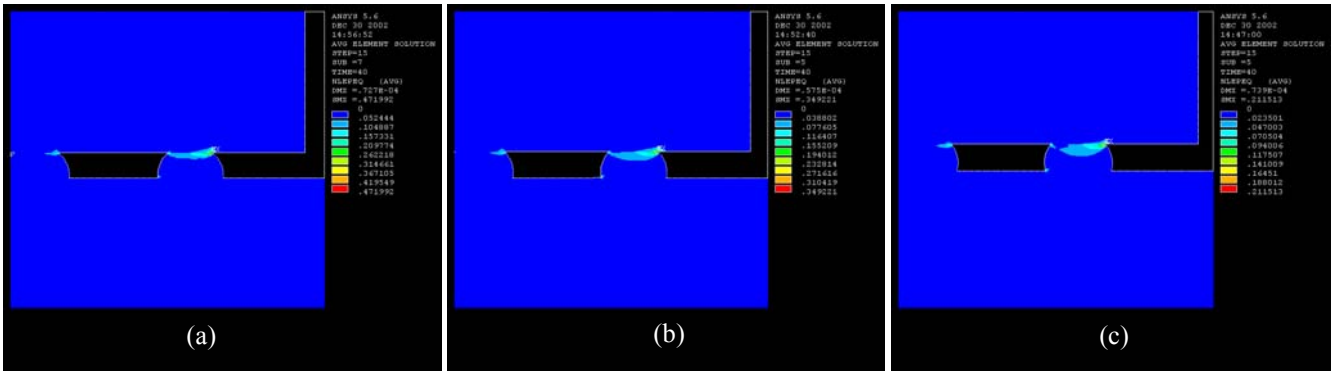


Fig. 19: Incremental equivalent plastic strain after five thermal cycles of (a) MPE002, (b) MPE003 and (c) MPE004

packages, therefore it shows the worst reliability.

As shown in Table 1, the UBM diameter of MPE004 is 100 μm, MPE003 is 90 μm and MPE002 is 80 μm. The substrate opening is 120um and the bump height after assembly is 80 μm in these three packages. Comparing these design parameters with thermal cycle testing and FEM results, it is obvious that the closer UBM diameter size to the substrate opening size, the better reliability of a flip chip packaging structure. And, it is believed that the reliability of the flip chip BGA package will upgrade if the solder bump heights can be fabricated to a higher value. To conclude, a proper selection of the pad opening size combination and the solder bump height can enhance the packaging reliability.

Ⅶ. Conclusions

In accordance with this investigation, the fine pitch flip chip BGA packages including daisy chain circuit are designed, fabricated and tested for the parametric reliability analysis. With the corresponding trend between thermal cycle testing, FEM simulation and analytical solution results, the following conclusions are addressed:

1. According to the thermal cycle testing and FEM simulation results, these parametric studies of the flip chip BGA packaging structures indicate that the reliability of a flip chip BGA package is highly related to the solder joint geometry if the other design parameters are fixed (package structure, solder joint layout, and material properties). Thereby, it could be concluded that a proper selection of the solder bump height and the pad size combination between the die side opening as well as substrate side opening can improve the solder bump shape and upgrade the packaging reliability.
2. Based on the analytical solder joint shape prediction algorithms: truncated sphere theory and the force-balanced method, the solder joint geometry after assembly can be predicted for a preliminary packaging reliability design consideration. Following the analysis of thermal cycle testing experiments and the FEM simulation results; it is found that the trends of the flip chip BGA packaging reliability coincide with the analytical solutions for solder joint shape prediction. Thus it is confirmed that the analytical methods of the solder joint shape prediction can be practically applied for the preliminary packaging reliability design consideration.

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